					Course Code:B23EC3101
SAGI RAMA KRISHNAM RAJU ENGINEERING COLLEGE (A)					**R23**
III B. Tech. I Semester MODEL QUESTION PAPER					
ANALOG AND DIGITAL IC APPLICATIONS					
For ECE					
Time: 3 Hrs.					**Max. Marks: 70 M**
Answer Question No.1 compulsorily					
Answer **ONE Question** from **EACH UNIT**					
Assume suitable data if necessary					
					10 x 2 = 20 Marks
			CO	**KL**	**M**
1.	**a).**	Draw the Pin diagram of Op-Amp.	**1**	**2**	**2**
	b).	Define CMRR.	**1**	**3**	**2**
	c).	Draw the circuit diagram of first order HPF using op-amp	**2**	**2**	**2**
	d).	Draw the circuit diagram of current to voltage converter using op-amp	**2**	**1**	**2**
	e).	Draw the Pin diagram of 555 timer.	**3**	**1**	**2**
	f).	Mention any 4 applications of 555 Timer as Monostable multivibrator.	**3**	**2**	**2**
	g).	What are the different types of DACs?	**4**	**2**	**2**
	h).	List important specifications of ADC.	**4**	**1**	**2**
	i).	Draw the circuit diagram of Decoder using 74x138.	**5**	**2**	**2**
	j).	Draw the Pin diagram of IC 7476.	**5**	**1**	**2**
					5 x 10 = 50 Marks
		UNIT-1			
2.	**a).**	Draw a block diagram of typical OP-AMP and explain the function of each block.	**1**	**3**	**5**
	b).	Explain the operation of Square wave generator circuit with neat circuit diagram and derive expression for time period.	**1**	**4**	**5**
		OR			
3.	**a).**	Explain the operation of a Regenerative comparator with circuit diagram and Waveforms.	**1**	**2**	**4**
	b).	Explain the operation of any 2 of the following op amp applications. (i) Differentiator (ii) Summing amplifier (iii) Logarithmic amplifier	**1**	**4**	**6**
		UNIT-2			
4.	**a).**	Derive the transfer function of a second order LPF. Comment on its frequency response.	**2**	**3**	**5**
	b).	Draw the basic circuit of an op amp based RC phase shift oscillator and explain its operation. Also, derive the expression for frequency of	**2**	**4**	**5**

		oscillation.			
		OR			
5.	**a).**	Design voltage to current converter using op-amp and then explain its operation.	**2**	**3**	**5**
	b).	Draw the op amp based bandpass filter circuit and briefly explain about its operating principle along with its frequency response curve.	**2**	**3**	**5**
		UNIT-3			
6.	**a).**	Draw the circuit of Schmitt trigger using IC555 timer and explain its operation?	**3**	**3**	**5**
	b).	Draw and explain the working of 555-timer circuit in astable mode to get output waveform with 50% duty cycle.	**3**	**4**	**5**
		OR			
7.	**a).**	List important specifications of 566 VCO IC.	**3**	**3**	**5**
	b).	With the help of schematic diagram of 555 timer, explain how it can be used as mono stablemultivibrator	**3**	**4**	**5**
		UNIT-4			
8.	**a).**	With a neat diagram explain the working principle of R-2R ladder type DAC.	**4**	**3**	**5**
	b).	With a neat block diagram, explain successive approximation type A/D converters in detail.	**4**	**3**	**5**
		OR			
9.	**a).**	Which is the fastest ADC? Explain the operation and discuss its merits and demerits.	**4**	**3**	**5**
	b).	Draw and explain the circuit diagram of parallel comparator type ADC.	**4**	**3**	**5**
		UNIT-5			
10.	**a).**	Design an asynchronous Decade counter using IC 7476 and explain the operation.	**5**	**4**	**5**
	b).	Explain the following Sequential logic circuits with suitable ICs. (a) Multiplexer. (b) Priority Encoder.	**5**	**3**	**5**
		OR			
11.	**a).**	Explain the following Combinational logic circuits with suitable ICs. (a) D flip-flop. (b) JK Flip-flop.	**5**	**3**	**5**
	b).	Design an Universal shift Register using IC74X194 and explain the operation.	**5**	**4**	**5**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE : Questions can be given as A,B splits or as a single Question for 10 marks

					Course Code: B23EC3102
		SAGI RAMA KRISHNAM RAJU ENGINEERING COLLEGE (A)			**R23**
		III B.Tech. I Semester MODEL QUESTION PAPER			
		ANTENNAS & WAVE PROPAGATION			
		For ECE			
Time: 3 Hrs.					**Max. Marks: 70 M**
		Answer Question No.1 compulsorily			
		Answer **ONE Question** from **EACH UNIT**			
		Assume suitable data if necessary			
					10 x 2 = 20 Marks
			CO	**KL**	**M**
1.	**a).**	Define Half Power Beam Width.	**1**	**2**	**2**
	b).	What is meant by Polarization? And its types.	**1**	**1**	**2**
	c).	List out the salient features of antenna array?	**2**	**2**	**2**
	d).	What is meant by array factor?	**2**	**1**	**2**
	e).	What are the advantages of microstrip antenna?	**3**	**1**	**2**
	f).	What is Spill over and back lobe radiation	**3**	**1**	**2**
	g).	What are the possible errors in antenna measurements?	**4**	**2**	**2**
	h).	What are the methods to measure Phase of an antenna?	**4**	**1**	**2**
	i).	Define wave tilt	**5**	**1**	**2**
	j).	Find the range of LOS system when they receive and transmit antenna heights are 10m and 100m respectively.	**5**	**3**	**2**
					5 x 10 = 50 Marks
		UNIT-1			
2.	**a).**	Derive expressions for the EM fields radiated by a λ/2 Dipole.	**1**	**3**	**5**
	b).	Discuss the Radiation characteristics of dipole antennas	**1**	**2**	**5**
		OR			
3.	**a).**	Compute the radiation resistance of a Quarter wave Monopole.	**1**	**3**	**5**
	b).	Explain about different types of current distribution on linear Antennas.	**1**	**2**	**5**
		UNIT-2			
4	**a)**	Obtain expressions for BWFN and HPBW in Broad-side array.	**2**	**3**	**5**
	b)	Show that in a Uniform linear array, the first side lobe is down the principal maximum by 13.5 db	**2**	**3**	**5**
		OR			
5.	**a)**	Derive the Electric field radiated by a two element uniform linear array.	**2**	**3**	**5**
	b)	Explain the technique of pattern multiplication with examples	**2**	**2**	**5**

		UNIT-3			
6.	**a).**	With a neat diagram, explain the operating principles of Log periodic Antenna. List out the disadvantages of a Log periodic Antenna	**3**	**2**	**5**
	b).	Obtain Design parameters of Yagi Uda antenna to operate at 30 MHz.	**3**	**4**	**5**
		OR			
7.	**a).**	Explain in detail the operating principles of Helical antenna.	**3**	**2**	**5**
	b).	Derive an expression for the expression of the impedance of the Slot Antenna.	**3**	**3**	**5**
		UNIT-4			
8.	**a).**	Explain in detail about the slotted line method of antenna input Impedance measurement.	**4**	**2**	**5**
	b).	Explain the method of measuring the radiation pattern of an antenna.	**4**	**2**	**5**
		OR			
9.	**a).**	Explain the measurement of antenna gain using two antenna method.	**4**	**2**	**5**
	b).	Explain the method of measurement of phase of an antenna.	**4**	**2**	**5**
		UNIT-5			
10.	**a).**	Derive an expression for the refractive index of the Ionosphere**.**	**5**	**2**	**5**
	b)	Explain ground wave propagation in detail.	**5**	**2**	**5**
		OR			
11.	**a).**	Derive an expression for the field strength of a Space wave.	**5**	**3**	**5**
	b).	Explain the terms Critical frequency, MUF and Skip distance.	**5**	**2**	**5**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE : Questions can be given as A,B splits or as a single Question for 10 marks

					Course Code: B23EC3103
		SAGI RAMA KRISHNAM RAJU ENGINEERING COLLEGE (A)			**R23**
		III B.Tech. I Semester MODEL QUESTION PAPER			
		DIGITAL COMMUNICATIONS			
		For ECE			
Time: 3 Hrs.					**Max. Marks: 70 M**
		Answer Question No.1 compulsorily			
		Answer **ONE Question** from **EACH UNIT**			
		Assume suitable data if necessary			
					10 x 2 = 20 Marks
			CO	**KL**	**M**
1.	**a).**	State Nyquist Sampling theorem.	**1**	**1**	**2**
	b).	What is companding?	**1**	**1**	**2**
	c).	What is bit rate?	**2**	**1**	**2**
	d).	Draw the phasor diagram for the QPSK system.	**2**	**1**	**2**
	e).	Define Noise bandwidth.	**3**	**1**	**2**
	f).	Show that the coefficients of spectral components a_k and b_k are uncorrelated to each other.	**3**	**2**	**2**
	g).	What is a matched filter?	**4**	**1**	**2**
	h).	What is a correlator?	**4**	**1**	**2**
	i).	List any two advantages of spread spectrum modulation.	**5**	**1**	**2**
	j).	List any two applications of spread spectrum modulation.	**5**	**1**	**2**
					5 x 10 = 50 Marks
		UNIT-I			
2.	**a).**	Explain how the linear delta modulation can be used for baseband signal transmission. What are the limitations and how can they be eliminated?	**1**	**2**	**5**
	b).	Explain the operation of Differential Pulse Code Modulation (DPCM) with neat block diagrams.	**1**	**2**	**5**
		OR			
3.	**a).**	Explain the operation of a PCM system with the help of a neat block diagram and an example.	**1**	**2**	**5**
	b).	With the help of an example, explain the operation of a synchronous TDM-PCM system(T1-Digital System).	**1**	**2**	**5**
		UNIT-II			
4.	**a).**	Explain the operation of Binary Phase Shift Keying(BPSK) system with the help of neat block diagrams.	**2**	**2**	**5**
	b).	Explain the operation of Minimum Shift Keying (MSK) with neat block diagrams. Sketch the MSK waveforms for the given bit stream b(t)=	**2**	**2**	**5**

		0110100 for m = 5.			
		OR			
5.	**a).**	Explain the operation of Quadrature Phase Shift Keying(QPSK) system with the help of neat block diagrams.	**2**	**2**	**5**
	b).	In a DEPSK Receiver, the received bit sequence b(t) is 01101100 then i) Find reconstructed bit sequence d(t) ii)Due to the presence of noise b(t) is recovered as 01111100 then, detect d(t) and also identify the bits which are wrongly detected. Use EX-OR logic.	**2**	**3**	**5**
		UNIT-III			
6.	**a).**	Explain about linear filtering and calculate noise power output of RC low pass filter and an integrator.	**3**	**2**	**5**
	b).	Explain about frequency domain representation of noise.	**3**	**2**	**5**
		OR			
7.	**a).**	Explain some sources of noise and narrow band representation of noise.	**3**	**2**	**5**
	b).	What is the effect of filtering on power spectral density of noise and obtain the relation between H(f), input noise PSD $G_{ni(f)}$ & output noise PSD $G_{no(f)}$	**3**	**2**	**5**
		UNIT-IV			
8.	**a).**	Explain the function of a baseband signal receiver and derive its probability of error?	**4**	**2**	**5**
	b).	By deriving expression for P_e for BPSK and BFSK systems, compare the performance of these two data transmission systems	**4**	**3**	**5**
		OR			
9.	**a).**	Derive an expression of Probability of error P_e for an optimum filter.	**4**	**3**	**5**
	b).	Derive the expression of Probability of error P_e for a matched filter.	**4**	**3**	**5**
		UNIT-V			
10.	**a).**	Derive an expression for output SNR when the binary signal is transmitted using BPSK in a PCM system.	**5**	**3**	**6**
	b).	Compare the noise performance of PCM and DM systems.	**5**	**3**	**4**
		OR			
11.	**a).**	How a CDMA system uses DS Spread Spectrum to provide multiple access communication.	**5**	**2**	**5**
	b).	Explain the operation of Frequency Hopping Spread Spectrum with the help of a neat block diagram.	**5**	**2**	**5**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE : Questions can be given as A,B splits or as a single Question for 10 marks

					Course Code: B23EC3104
SAGI RAMA KRISHNAM RAJU ENGINEERING COLLEGE (A)					**R23**
III B.Tech. I Semester MODEL QUESTION PAPER					
CMOS Digital Integrated Circuits Analysis and Design					
For ECE					
Time: 3 Hrs.					**Max. Marks: 70 M**
Answer Question No.1 compulsorily					
Answer **ONE Question** from **EACH UNIT**					
Assume suitable data if necessary					
					10 x 2 = 20 Marks
			CO	**KL**	**M**
1.	**a).**	What are the key components of a MOS structure?	**1**	**1**	**2**
	b).	Differentiate between full-custom and semi-custom VLSI design.	**1**	**2**	**2**
	c).	What is the purpose of oxidation in MOSFET fabrication?	**2**	**2**	**2**
	d).	Draw the basic layout structure of a NAND2 gate.	**2**	**3**	**2**
	e).	What is propagation delay in a digital circuit?	**3**	**1**	**2**
	f).	What is short-circuit power dissipation in a CMOS inverter?	**3**	**2**	**2**
	g).	Why are sequential circuits used in digital design?	**4**	**2**	**2**
	h).	What is the function of a D-latch?	**4**	**1**	**2**
	i).	How does volatile memory differ from non-volatile memory?	**5**	**2**	**2**
	j).	What is the role of the capacitor in a DRAM cell?	**5**	**2**	**2**
					5 x 10 = 50 Marks
		UNIT-1			
2.	**a).**	Explain the structure and working principle of a Metal-Oxide-Semiconductor (MOS) capacitor.	**1**	**2**	**6**
	b).	Discuss the small-geometry effects in MOSFETs and their influence on circuit behavior.	**1**	**3**	**4**
		OR			
3.	**a).**	Describe the different steps involved in the VLSI design flow with a suitable block diagram.	**1**	**3**	**6**
	b).	Compare the advantages and disadvantages of resistive-load inverters.	**1**	**4**	**4**
		UNIT-2			
4.		Describe the fabrication process flow of CMOS technology with necessary diagrams.	**2**	**3**	**10**
		OR			
5.	**a).**	Design and explain the layout of a 2-input NAND gate using CMOS technology.	**2**	**3**	**6**
	b).	Draw a layout for the CMOS Inverter.	**2**	**3**	**4**

		UNIT-3			
6.	**a).**	Discuss the factors affecting the switching speed of MOS circuits.	**3**	**4**	**5**
	b).	Define propagation delay, rise time, and fall time in digital circuits. Explain their significance.	**3**	**2**	**5**
		OR			
7.	**a).**	Describe different methods for estimating interconnect parasitics in VLSI design.	**3**	**3**	**5**
	b).	Explain different types of power dissipation in CMOS inverters.	**3**	**2**	**5**
		UNIT-4			
8.	**a).**	What are bi-stable elements? Explain their behavior with state diagrams.	**4**	**2**	**5**
	b).	What are the limitations of an SR latch, and how are they overcome?	**4**	**4**	**5**
		OR			
9.	**a).**	Describe the working of a CMOS D-latch with circuit diagram and timing waveforms.	**4**	**3**	**5**
	b).	What is time borrowing in sequential circuits? Explain with an example.	**4**	**3**	**5**
		UNIT-5			
10.		Describe the working principle of an SRAM cell with a circuit diagram.	**5**	**3**	**10**
		OR			
11.		Explain the basic structure and working of a DRAM cell with a suitable diagram.	**5**	**3**	**10**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE : Questions can be given as A,B splits or as a single Question for 10 marks

					Course Code: B23EC3105
SAGI RAMA KRISHNAM RAJU ENGINEERING COLLEGE (A)					**R23**
III B.Tech. I Semester MODEL QUESTION PAPER					
ELECTRONICMEASUREMENTS ANDINSTRUMENTATION					
For ECE					
Time: 3 Hrs.					**Max. Marks: 70 M**
Answer Question No.1 compulsorily					
Answer **ONE Question** from **EACH UNIT**					
Assume suitable data if necessary					
					10 x 2 = 20 Marks
			CO	**KL**	**M**
1.	**a).**	What is meant by accuracy and precision in measurement?	**1**	**2**	**2**
	b).	Define and explain types of static errors.	**1**	**2**	**2**
	c).	What is a transducer? Give two examples.	**2**	**2**	**2**
	d).	Define active and passive transducers with examples.	**2**	**2**	**2**
	e).	What is an oscilloscope? Mention its basic purpose.	**3**	**2**	**2**
	f).	Define trigger pulse and sweep in CRO.	**3**	**2**	**2**
	g).	What is the purpose of using a Wheatstone bridge?	**4**	**2**	**2**
	h).	Write the applications of capacitance bridges.	**4**	**2**	**2**
	i).	What is a signal generator? Mention its use.	**5**	**2**	**2**
	j).	Define harmonic distortion analyzer.	**5**	**2**	**2**
					5 x 10 = 50 Marks
		UNIT-1			
2.	**a).**	Define resolution and sensitivity in electronic instruments.	**1**	**3**	**5**
	b).	What is the significance of fidelity and lag in dynamic characteristics?	**1**	**3**	**5**
		OR			
3.	**a).**	List the types of DC and AC voltmeters and mention one application each.	**1**	**3**	**5**
	b).	Describe the working of a True RMS voltmeter.	**1**	**4**	**5**
		UNIT-2			
4.	**a).**	What are active and passive transducers? Give one example each.	**2**	**2**	**5**
	b).	State the principle of a piezoelectric transducer.	**2**	**2**	**5**
		OR			
5.	**a).**	What is a strain gauge? List two types.	**2**	**2**	**5**
	b).	How does a resistance thermometer measure temperature?	**2**	**3**	**5**
		UNIT-3			

6.	**a).**	Define sweep and trigger pulse in CRO.	**3**	**2**	**5**
	b).	What is a dual trace oscilloscope?	**3**	**2**	**5**
		OR			
7.	**a).**	List the features of a digital storage oscilloscope.	**3**	**3**	**5**
	b).	How is frequency measured using Lissajous patterns?	**3**	**3**	**5**
		UNIT-4			
8.	**a).**	What is the purpose of a Wheatstone bridge?	**4**	**2**	**5**
	b).	List the precautions to be taken while using electrical bridges.	**4**	**2**	**5**
		OR			
9.	**a).**	Define the principle of a Schering bridge.	**4**	**2**	**5**
	b).	Mention one application each for inductance and capacitance bridges.	**4**	**3**	**5**
		UNIT-5			
10.	**a).**	List different types of signal generators and their outputs.	**5**	**3**	**5**
	b).	What is an arbitrary waveform generator?	**5**	**3**	**5**
		OR			
11.	**a).**	Differentiate between sine wave and square wave signal generators.	**5**	**3**	**5**
	b).	Define sweep generator and mention its use.	**5**	**4**	**5**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE : Questions can be given as A,B splits or as a single Question for 10 marks

					Course Code: B23EC3106
		SAGI RAMA KRISHNAM RAJU ENGINEERING COLLEGE (A)			**R23**
		III B.Tech. I Semester MODEL QUESTION PAPER			
		BIO-MEDICAL INSTRUMENTATION			
		For ECE			
Time: 3 Hrs.					**Max. Marks: 70 M**
		Answer Question No.1 compulsorily			
		Answer **ONE Question** from **EACH UNIT**			
		Assume suitable data if necessary			
					10 x 2 = 20 Marks
			CO	**KL**	**M**
1.	**a).**	What are the basic objectives of a medical instrumentation system?	**1**	**2**	**2**
	b).	Define resting and action potentials.	**1**	**2**	**2**
	c).	Define ECG and mention its importance.	**2**	**2**	**2**
	d).	What are the components of the cardiovascular system?	**2**	**2**	**2**
	e).	What is intensive care monitoring?	**3**	**2**	**2**
	f).	List any two instruments used in respiratory system analysis.	**3**	**2**	**2**
	g).	What is bio-telemetry?	**4**	**2**	**2**
	h).	Name any two physiological parameters suitable for bio-telemetry.	**4**	**2**	**2**
	i).	What is the purpose of X-ray instrumentation in medical diagnostics?	**5**	**2**	**2**
	j).	Define electrical shock hazard.	**5**	**2**	**2**
					5 x 10 = 50 Marks
		UNIT-1			
2.	**a).**	List the major physiological systems of the human body.	**1**	**2**	**5**
	b).	What is the role of electrodes in biomedical instrumentation?	**1**	**2**	**5**
		OR			
3.	**a).**	Explain the significance of biomedical signals.	**1**	**2**	**5**
	b).	Mention any two types of bio-potential electrodes.	**1**	**2**	**5**
		UNIT-2			
4.	**a).**	Explain the working principle of a blood pressure measurement system.	**2**	**3**	**5**
	b).	What is the significance of PQRS and T waves in ECG?	**2**	**3**	**5**
		OR			
5.	**a).**	Define cardiac output and its measurement method.	**2**	**2**	**5**
	b).	What is plethysmography?	**2**	**2**	**5**
		UNIT-3			
6.	**a).**	What is the function of a pacemaker?	**3**	**2**	**5**

	b).	What are the elements of patient monitoring equipment?	**3**	**2**	**5**
		OR			
7.	**a).**	How is respiration analyzed in biomedical systems?	**3**	**3**	**5**
	b).	Explain the need for calibration in patient monitoring systems.	**3**	**3**	**5**
		UNIT-4			
8.	**a).**	List the main components of a bio-telemetry system.	**4**	**2**	**5**
	b).	What are implantable telemetry units?	**4**	**3**	**5**
		OR			
9.	**a).**	Mention any two tests carried out on blood in clinical laboratories.	**4**	**2**	**5**
	b).	What is the role of automation in clinical testing?	**4**	**3**	**5**
		UNIT-5			
10.	**a).**	List the physiological effects of electrical current on the human body.	**5**	**2**	**5**
	b).	What is medical thermography used for?	**5**	**3**	**5**
		OR			
11.	**a).**	Name any two modern imaging techniques.	**5**	**2**	**5**
	b).	What methods are used for electrical accident prevention in hospitals?	**5**	**3**	**5**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE : Questions can be given as A,B splits or as a single Question for 10 marks

					Course Code: B23EC3107
		SAGI RAMA KRISHNAM RAJU ENGINEERING COLLEGE (A)			**R23**
		III B.Tech. I Semester MODEL QUESTION PAPER			
		DIGITAL SYSTEM DESIGN			
		For ECE			
Time: 3 Hrs.					**Max. Marks: 70 M**
		Answer Question No.1 compulsorily			
		Answer **ONE Question** from **EACH UNIT**			
		Assume suitable data if necessary			
					10 x 2 = 20 Marks
			CO	**KL**	**M**
1.	**a).**	What is the role of a module in Verilog HDL?	**1**	**2**	**2**
	b).	Define gate primitives in Verilog with one example.	**1**	**2**	**2**
	c).	What is a procedural assignment in Verilog behavioral modeling?	**2**	**2**	**2**
	d).	Differentiate between sequential and parallel blocks.	**2**	**2**	**2**
	e).	What is a continuous assignment in dataflow modeling?	**3**	**2**	**2**
	f).	List any two operators used in Verilog dataflow model.	**3**	**2**	**2**
	g).	What is the difference between Moore and Mealy machines?	**4**	**2**	**2**
	h).	Define a user-defined primitive (UDP) with a basic example.	**4**	**2**	**2**
	i).	What is a test bench in Verilog?	**5**	**2**	**2**
	j).	Define design verification.	**5**	**2**	**2**
					5 x 10 = 50 Marks
		UNIT-1			
2.	**a).**	List different data types used in Verilog.	**1**	**2**	**5**
	b).	What are system tasks in Verilog? Give examples.	**1**	**2**	**5**
		OR			
3.	**a).**	Explain the purpose of tri-state gates in digital design.	**1**	**2**	**5**
	b).	What is the use of delay specification in gate-level modeling?	**1**	**2**	**5**
		UNIT-2			
4.	**a).**	What is the role of loops in behavioral modeling?	**2**	**2**	**5**
	b).	Explain conditional statements used in Verilog.	**2**	**2**	**5**
		OR			
5.	**a).**	How is a flip-flop designed using behavioral modeling?	**2**	**3**	**5**
	b).	Write a simple Verilog code for a 4-to-1 multiplexer using behavioral model.	**2**	**3**	**5**
		UNIT-3			

6.	**a).**	How are delays specified in continuous assignments?	**3**	**2**	**5**
	b).	Write a simple Verilog code for a decoder using dataflow modeling.	**3**	**3**	**5**
		OR			
7.	**a).**	What are the basic transistor switches used in switch-level modeling?	**3**	**2**	**5**
	b).	Differentiate between dataflow and behavioral modeling.	**3**	**3**	**5**
		UNIT-4			
8.	**a).**	What are the basic components of a state machine?	**4**	**2**	**5**
	b).	Write the advantages of using one-hot encoding in FSM design.	**4**	**2**	**5**
		OR			
9.	**a).**	What is the purpose of synthesis in digital design?	**4**	**3**	**5**
	b).	Explain the synthesis of sequential logic using flip-flops.	**4**	**3**	**5**
		UNIT-5			
10.	**a).**	Explain the purpose of assertion verification.	**5**	**2**	**5**
	b).	How are combinational circuits tested using a test bench?	**5**	**2**	**5**
		OR			
11.	**a).**	Mention two techniques for testing sequential circuits.	**5**	**3**	**5**
	b).	Write a simple Verilog test bench to verify a 2-input AND gate.	**5**	**3**	**5**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE : Questions can be given as A,B splits or as a single Question for 10 marks

					Course Code: B23EC3108
		SAGI RAMA KRISHNAM RAJU ENGINEERING COLLEGE (A)			**R23**
		III B.Tech. I Semester MODEL QUESTION PAPER			
		ARTIFICIAL INTELLIGENCE			
		For ECE			
Time: 3 Hrs.					**Max. Marks: 70 M**
		Answer Question No.1 compulsorily			
		Answer **ONE Question** from **EACH UNIT**			
		Assume suitable data if necessary			
					10 x 2 = 20 Marks
			CO	**KL**	**M**
1.	**a).**	What are AI techniques?	**1**	**2**	**2**
	b).	Define state space search with an example.	**1**	**2**	**2**
	c).	What is the difference between procedural and declarative knowledge?	**2**	**2**	**2**
	d).	Define predicate logic with an example.	**2**	**2**	**2**
	e).	Define non-monotonic reasoning.	**3**	**2**	**2**
	f).	State Bayes' theorem in the context of AI.	**3**	**2**	**2**
	g).	Define semantic nets with an example.	**4**	**2**	**2**
	h).	What is fuzzy logic? Mention one application.	**4**	**2**	**2**
	i).	What is the Mini-Max algorithm in game playing?	**5**	**2**	**2**
	j).	Define natural language processing (NLP).	**5**	**2**	**2**
					5 x 10 = 50 Marks
		UNIT-1			
2.	**a).**	Explain the characteristics of a production system.	**1**	**2**	**5**
	b).	What is generate-and-test method?	**1**	**2**	**5**
		OR			
3.	**a).**	Describe the concept of hill climbing search.	**1**	**3**	**5**
	b).	What is meant by means-ends analysis?	**1**	**3**	**5**
		UNIT-2			
4.	**a).**	What are Isa and instance relationships?	**2**	**2**	**5**
	b).	Distinguish between procedural and declarative knowledge.	**2**	**3**	**5**
		OR			
5.	**a).**	Explain simple fact representation in predicate logic.	**2**	**3**	**5**
	b).	What is logic programming in knowledge representation?	**2**	**3**	**5**
		UNIT-3			
6.	**a).**	Explain the concept of statistical reasoning.	**3**	**2**	**5**

	b).	What are Bayesian networks used for?	**3**	**3**	**5**
		OR			
7.	**a).**	Define Dempster-Shafer theory.	**3**	**3**	**5**
	b).	Differentiate between rule-based and probabilistic reasoning.	**3**	**3**	**5**
		UNIT-4			
8.	**a).**	What are frames in AI knowledge representation?	**4**	**2**	**5**
	b).	Explain the concept of conceptual dependency.	**4**	**3**	**5**
		OR			
9.	**a).**	What are scripts in slot-and-filler structures?	**4**	**2**	**5**
	b).	Compare weak and strong slot-filler structures.	**4**	**3**	**5**
		UNIT-5			
10.	**a).**	What is alpha-beta cut-off in game search?	**5**	**3**	**5**
	b).	List any two components of a planning system.	**5**	**2**	**5**
		OR			
11.	**a).**	What is the function of the Hopfield network?	**5**	**3**	**5**
	b).	Distinguish between symbolic AI and connectionist AI.	**5**	**3**	**5**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE : Questions can be given as A,B splits or as a single Question for 10 marks

				Course Code: B23EC1101	
		SAGI RAMA KRISHNAM RAJU ENGINEERING COLLEGE (A)			**R23**
		III B.Tech. II Semester MODEL QUESTION PAPER			
		VLSI DESIGN			
		For ECE			
Time: 3 Hrs.				**Max. Marks: 70 M**	
		Answer Question No.1 compulsorily			
		Answer **ONE Question** from **EACH UNIT**			
		Assume suitable data if necessary			
				10 x 2 = 20 Marks	
			CO	**KL**	**M**
1.	**a).**	What is the relation between I_{DS} and V_{DS} in MOSFET?	**1**	**2**	**2**
	b).	What is latch-up in CMOS circuits?	**1**	**2**	**2**
	c).	What is the purpose of using stick diagrams?	**2**	**2**	**2**
	d).	Draw the layout for the CMOS Inverter?	**2**	**3**	**2**
	e).	Define propagation delay in a CMOS inverter.	**3**	**1**	**2**
	f).	What is scaling and limitations of scaling?	**3**	**1**	**2**
	g).	List two static properties of Complementary CMOS.	**4**	**1**	**2**
	h).	What is the basic principle of Dynamic CMOS logic?	**4**	**2**	**2**
	i).	What is the significance of LUTs in FPGA?	**5**	**2**	**2**
	j).	Define Level Sensitive Scan Design (LSSD).	**5**	**1**	**2**
				5 x 10 = 50 Marks	
		UNIT-1			
2.	**a).**	Explain the CMOS fabrication steps with neat diagram?	**1**	**3**	**6**
	b).	Compare CMOS, Bi-CMOS and Bipolar Technologies?	**1**	**3**	**4**
		OR			
3.	**a).**	Illustrate the different forms of pull-up transistors in MOS inverter circuits. Also provide the voltage transfer characteristics for each of them?	**1**	**3**	**6**
	b).	What is latch-up in CMOS circuits? Explain its causes, effects, and prevention techniques?	**1**	**2**	**4**
		UNIT-2			
4.	**a).**	Draw the Stick Diagram of 2 input NOR gate using CMOS logic?	**2**	**3**	**6**
	b).	Explain about the Lambda based design rules for Transistor?	**2**	**2**	**4**
		OR			
5.	**a).**	Explain 2µm CMOS design rule for wires?	**2**	**2**	**6**
	b).	Explain about double poly CMOS rules?	**2**	**3**	**4**

		UNIT-3			
6.	**a).**	Explain the concept of sheet resistance (Rs) and how it is applied to MOS transistors and inverters?	**3**	**3**	**6**
	b).	Discuss limitations of scaling. Explain it on the substrate doping?	**3**	**3**	**4**
		OR			
7.	**a).**	What are inverter delays? Explain the factors that contribute to propagation delay in CMOS inverters?	**3**	**2**	**6**
	b).	Explain about limits due to sub threshold currents?	**3**	**3**	**4**
		UNIT-4			
8.	**a).**	Explain the working principle of Complementary CMOS logic. What are its key static properties?	**4**	**3**	**5**
	b).	Realize the implementation of two-input NOR gate using CMOS logic. Explain the associated operation by giving truth table?	**4**	**3**	**5**
		OR			
9.	**a).**	Design and Explain Multiplexer based Latches?	**4**	**2**	**6**
	b).	What is Pass Transistor Logic? Explain how logic gates can be designed using pass transistors?	**4**	**4**	**4**
		UNIT-5			
10.	**a).**	Explain Basic architecture of FPGA in detail?	**5**	**3**	**5**
	b).	Explain the key features of the Xilinx XC4000 FPGA family. How does it differ from other FPGA families?	**5**	**2**	**5**
		OR			
11.	**a).**	Explain logical stuck-at-0 or stuck-at-1 faults with the help of suitable examples?	**5**	**3**	**6**
	b).	Explain Built-In-Self Test (BIST) with the help of example?	**5**	**2**	**4**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE : Questions can be given as A,B splits or as a single Question for 10 marks

					Course Code: B23EC3202
		SAGI RAMA KRISHNAM RAJU ENGINEERING COLLEGE (A)			**R23**
		III B.Tech. II Semester MODEL QUESTION PAPER			
		DIGITAL SIGNAL PROCESSING			
		For ECE			
Time: 3 Hrs.					**Max. Marks: 70 M**
		Answer Question No.1 compulsorily			
		Answer **ONE Question** from **EACH UNIT**			
		Assume suitable data if necessary			
					10 x 2 = 20 Marks
			CO	**KL**	**M**
1.	**a).**	If X(z) is the z-transform of the signal x(n) then what is the ZT of anu(n) ?	**1**	**2**	**2**
	b).	Evaluate the Z-transform of $e^{3n}u(n)$?	**1**	**2**	**2**
	c).	What is the ROC of the z-transform of the signal x(n)=anu(n)+bnu(-n-1)	**2**	**2**	**2**
	d).	What is the DFT of the four-point sequence x(n)= {0,1,2,3}	**2**	**2**	**2**
	e).	What is the circular convolution of the sequences $X_1(n)$={2,1,2,1} and $x_2(n)$={1,2,3,4}	**3**	**1**	**2**
	f).	What is the cut-off frequency of the Butterworth filter with a pass band gain p=-1 dB at p=4 rad/sec and stop band attenuation greater than or equal to 20dB at s=8 rad/sec?	**3**	**2**	**2**
	g).	List out the expressions for Hanning and Blackman window functions.	**4**	**2**	**2**
	h).	Illustrate the criteria for selecting window functions used in FIR filter design?	**4**	**1**	**2**
	i).	Which operation has to be performed to increase the sampling rate by an integer factor L?	**5**	**1**	**2**
	j).	Discuss about anti aliasing filter?	**5**	**1**	**2**
					5 x 10 = 50 Marks
		UNIT-1			
2.	**a).**	Find the Z-transform of the signal x(n)=2n u(n)+3nu(-n-1) and its region of convergence.	**1**	**3**	**5**
	b).	Realize the series canonical realization of the following digital transfer function $X(Z) = \frac{z^2 + 2z + 4}{(z-8)(z^2 - 0.9z + 0.14)}$	**1**	**2**	**5**
		OR			
3.	**a).**	Compute the response of the following system to the input u(n). Discuss the stability of the given DT system?y(n)=0.7y(n-1)-0.12y(n-	**1**	**2**	**5**

		2)+x(n-1)+x(n-2)			
	b).	Find inverse Z-Transform of Find inverse Z-Transform of X(z)=(z^2+2z+3)/(z-1)(z-3)(z-4) for i) |z|>4 ii) |z|<1	**1**	**4**	**5**
		UNIT-2			
4.		Compute the DFT of the following sequence using Radix–2 DIT FFT algorithm. Show the all intermediate stage results: x(n)={0,1,2,0,2,1,0,2}	**2**	**3**	**10**
		OR			
5.		Obtain circular convolution of the two sequences given below using DFT approach x(n)={0,1,0,0}, h(n)={2,2,2,2}	**2**	**3**	**10**
		UNIT-3			
6.		Design digital Butterworth lowpass IIR filter using BLT method. The filter specifications are given by i) -3dB cutoff frequency at 0.5π rad, ii) at least 15dB attenuation at 0.75π rad	**3**	**4**	**10**
		OR			
7.	**a).**	Compare Chebyshev and Butterworth analog filters?	**3**	**4**	**5**
	b).	Convert the following analog filter with transfer function using impulse invariance method. HaS=s+0.2s+0.2)2+25	**3**	**4**	**5**
		UNIT-4			
8.		Design a linear-phase low pass FIR digital filter to meet the following specifications: (i) Pass band = 0 to 10 kHz (ii) Sampling frequency = 100 kHz, N=11. Compute the impulse response and transfer function of the desired FIR digital filter using Hamming window?	**4**	**3**	**10**
		OR			
9.	**a).**	Compare IIR and FIR digital filters?	**4**	**3**	**5**
	b).	Show that FIR filters provide constant group delay and phase delay?	**4**	**4**	**5**
		UNIT-5			
10.		Illustrate the operation of up-sampler, down-sampler, Interpolator and Decimator in time and frequency domains with neat sketches.	**5**	**4**	**10**
		OR			
11.	**a).**	Explain how Sub band coding of speech signals reduces the bit rate**.**	**5**	**3**	**5**
	b).	Discuss the effects of finite word length registers.	**5**	**4**	**5**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE : Questions can be given as A,B splits or as a single Question for 10 marks

		Course Code: B23EC3201			
		SAGI RAMA KRISHNAM RAJU ENGINEERING COLLEGE (A)			**R23**
		III B.Tech. II Semester MODEL QUESTION PAPER			
		MICROPROCESSORS AND MICROCONTROLLERS			
		Electronics and Communication Engineering			
Time: 3 Hrs.					**Max. Marks: 70 M**
		Answer Question No.1 compulsorily			
		Answer **ONE Question** from **EACH UNIT**			
		Assume suitable data if necessary			
					10 x 2 = 20 Marks
			CO	**KL**	**M**
1.	**a).**	What are the three groups of signals in 8086?	**1**	**1**	**2**
	b).	What are the advantages of segmented memory?	**1**	**1**	**2**
	c).	Explain the difference between the ADD and ADDC instructions.	**2**	**1**	**2**
	d).	Give the register classification of 8086.	**2**	**1**	**2**
	e).	What is the significance of EA bar pin in 8051?	**3**	**1**	**2**
	f).	Explain PSW register?	**3**	**2**	**2**
	g).	Explain the role of the C/T bit in the TMOD register.	**4**	**2**	**2**
	h).	List the modes of timer in 8051.	**4**	**2**	**2**
	i).	Give different applications of ARM processors.	**5**	**1**	**2**
	j).	What is "Thumb" in ARM processor?	**5**	**1**	**2**
					5 x 10 = 50 Marks
		UNIT-1			
2.		Draw and explain the functional block diagram INTEL 8086 Microprocessor.	**1**	**3**	**10**
		OR			
3.	**a).**	Illustrate the generation of a 20-bit physical address in 8086 with an example.	**1**	**3**	**5**
	b).	Draw the flag register of 8086 and explain the function of each flag in detail.	**1**	**2**	**5**
		UNIT-2			
4.	**a).**	Draw the programmable register array of 8086 and explain the function of each Register.	**2**	**2**	**5**
	b).	Write an 8086-assembly language program to find the largest byte for a given block of bytes.	**2**	**4**	**5**
		OR			
5.	**a).**	Explain addressing modes of 8086 with suitable example.	**2**	**3**	**5**
	b).	Write an assembly language program for 8086 to find if given number is even or odd.	**2**	**3**	**5**

		UNIT-3			
6.		Outline the features and explain the internal block diagram of 8051 microcontroller.	**3**	**3**	**10**
		OR			
7.	**a).**	Explain memory organization in 8051 Microcontroller.	**3**	**2**	**5**
	b).	Classify the instructions of 8051 Microcontroller and Explain basic arithmetic Instructions.	**3**	**2**	**5**
		UNIT-4			
8.	**a).**	Explain TMOD and TCON register.	**4**	**2**	**5**
	b).	Explain Mode-1 programming of 8051 timer. Describe the different steps to program in Mode-1.	**4**	**3**	**5**
		OR			
9.	**a).**	With neat diagram write an assembly language program to interface ADC0808 to 8051 microcontrollers.	**4**	**3**	**5**
	b).	Write an assembly language program to generate a square wave on port pin P1.2 of 1kHz using timer-0 in mode 2.	**4**	**3**	**5**
		UNIT-5			
10.	**a).**	Explain the various ARM families and their features.	**5**	**3**	**5**
	b).	Explain ARM core dataflow model with a neat diagram.	**5**	**3**	**5**
		OR			
11.	**a).**	With a neat diagram explain the different general purpose registers of ARM processors.	**5**	**2**	**5**
	b).	Explain current program status register (CPSR) with neat diagram.	**5**	**2**	**5**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE : Questions can be given as A,B splits or as a single Question for 10 marks

					Course Code: B23EC3204
		SAGI RAMA KRISHNAM RAJU ENGINEERING COLLEGE (A)			**R23**
		III B.Tech. II Semester MODEL QUESTION PAPER			
		ADVANCED DIGITAL LOGIC DESIGN AND PROTOTYPING ON FPGA			
		For ECE			
Time: 3 Hrs.					**Max. Marks: 70 M**
		Answer Question No.1 compulsorily			
		Answer **ONE Question** from **EACH UNIT**			
		Assume suitable data if necessary			
					10 x 2 = 20 Marks
			CO	**KL**	**M**
1.	**a).**	Define a logic gate. Give examples.	**1**	**2**	**2**
	b).	What is the difference between latch and flip-flop?	**1**	**2**	**2**
	c).	Differentiate between Mealy and Moore machines.	**2**	**3**	**2**
	d).	What is state encoding in FSMs?	**2**	**3**	**2**
	e).	What do you mean by "low power FSM"?	**3**	**4**	**2**
	f).	List any two real-time applications of FSMs.	**3**	**4**	**2**
	g).	Define JTAG. What is its role in FPGA programming?	**4**	**2**	**2**
	h).	Mention any two common programming methods used for FPGAs.	**4**	**2**	**2**
	i).	Mention any two examples of vendor-specific IP cores.	**5**	**3**	**2**
	j).	Name any two debugging tools used in FPGA design.	**5**	**3**	**2**
					5 x 10 = 50 Marks
		UNIT-1			
2.	**a).**	Explain the design and operation of basic logic gates using truth tables and Boolean expressions.	**1**	**2**	**6**
	b).	Design a combinational circuit for a 2-bit comparator and explain.	**1**	**2**	**4**
		OR			
3.	**a).**	Describe the working of an arithmetic logic unit (ALU) with block diagram.	**1**	**2**	**6**
	b).	Explain the operation of SR, JK, D, and T flip-flops with truth tables and logic diagrams.	**1**	**2**	**4**
		UNIT-2			
4.	**a).**	Explain the structure and working of a Mealy Machine with an example and state diagram.	**2**	**3**	**6**
	b).	What is state encoding? Explain different state encoding techniques (binary, one-hot, gray code) with suitable examples.	**2**	**3**	**4**
		OR			
5.	**a).**	Design a Moore FSM to detect the sequence “1101”. Draw the state diagram and transition table.	**2**	**3**	**6**
	b).	Describe the steps involved in designing a FSM from a given problem statement.	**2**	**3**	**4**

		UNIT-3			
6.	**a).**	Design a FSM-based vending machine that accepts ₹1 and ₹2 coins and dispenses a product for ₹5. Provide state diagram and Verilog code.	**3**	**4**	**10**
		OR			
7.	**a).**	What are low power FSMs? Discuss the techniques used to reduce power in FSM design (e.g., clock gating, state encoding).	**3**	**4**	**6**
	b).	Explain the benefits and challenges of implementing FSMs in hardware using HDL (Verilog/VHDL).	**3**	**4**	**4**
		UNIT-4			
8.	**a).**	Explain the architecture of a typical FPGA. Describe the role of CLBs, I/O blocks, and interconnects.	**4**	**2**	**5**
	b).	Explain the basic components and features of an FPGA development board. Use examples like Xilinx or Intel (Altera) boards.	**4**	**2**	**5**
		OR			
9.	**a).**	Explain the importance of programming interfaces in FPGA-based digital design. Discuss UART, USB, and JTAG interfaces in this context.	**4**	**2**	**10**
		UNIT-5			
10.	**a).**	Describe the process of integrating and customizing IP cores in a typical FPGA design flow using vendor tools.	**5**	**3**	**5**
	b).	Compare custom IP cores vs vendor-supplied IP cores in terms of flexibility, optimization, and portability.	**5**	**3**	**5**
		OR			
11.	**a).**	Describe FPGA prototyping methodologies with emphasis on their advantages for SoC/ASIC design validation.	**5**	**3**	**6**
	b).	Explain the steps for testing and debugging an FPGA-based system using simulation tools and on-board debugging resources.	**5**	**3**	**4**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE : Questions can be given as A,B splits or as a single Question for 10 marks

					Course Code: B23EC3205
SAGI RAMA KRISHNAM RAJU ENGINEERING COLLEGE (A)					**R23**
III B.Tech. II Semester MODEL QUESTION PAPER					
EMBEDDED SYSTEMS WITH ARM CORTEX-M3					
For ECE					
Time: 3 Hrs.					**Max. Marks: 70 M**
Answer Question No.1 compulsorily					
Answer **ONE Question** from **EACH UNIT**					
Assume suitable data if necessary					
					10 x 2 = 20 Marks
			CO	**KL**	**M**
1.	**a).**	List two key characteristics of embedded systems.	**1**	**1**	**2**
	b).	Differentiate between Harvard and Von Neumann architectures.	**1**	**2**	**2**
	c).	What is the purpose of special registers in Cortex-M3?	**2**	**2**	**2**
	d).	Explain the significance of the memory map in Cortex-M3 architecture.	**2**	**2**	**2**
	e).	What is the difference between an interrupt and an exception?	**3**	**1**	**2**
	f).	How does NVIC help in reducing interrupt latency?	**3**	**3**	**2**
	g).	Define instruction syntax	**4**	**1**	**2**
	h).	What is the role of CMSIS in embedded system development?	**4**	**2**	**2**
	i).	What is an RTOS, and why is it used in embedded systems?	**5**	**1**	**2**
	j).	What are the different debug modes available in ARM Cortex-M3?	**5**	**1**	**2**
					5 x 10 = 50 Marks
		UNIT-1			
2.	**a).**	Describe the RISC architecture and justify its use in ARM-based embedded systems.	**1**	**3**	**5**
	b).	Identify and explain the major challenges faced in embedded system design and development.	**1**	**2**	**5**
		OR			
3.	**a).**	Why is power efficiency crucial in embedded systems? Suggest techniques to reduce power consumption.	**1**	**2**	**5**
	b).	Describe various real-life applications of embedded systems across different domains.	**1**	**2**	**5**
		UNIT-2			
4.		Describe the architecture of Cortex-M3 with a labeled block diagram. Explain the role of each component	**2**	**2**	**10**
		OR			
5.	**a).**	Explain the different operation modes of Cortex-M3 and their significance in embedded applications.	**2**	**1**	**5**

	b).	Describe the pipeline mechanism in Cortex-M3. How does it improve instruction execution?	**2**	**2**	**5**
		UNIT-3			
6.		How does Direct Memory Access (DMA) reduce CPU workload? Discuss its advantages.	**3**	**3**	**10**
		OR			
7.	**a).**	What is the role of the Nested Vectored Interrupt Controller (NVIC)? Explain its features.	**3**	**2**	**5**
	b).	Describe the complete interrupt/exception sequence in Cortex-M3.	**3**	**2**	**5**
		UNIT-4			
8.	**a).**	Explain the concept of interrupt latency and the factors affecting it.	**4**	**2**	**5**
	b).	Evaluate the benefits of automatic stacking and unstacking during an exception in Cortex-M3.	**4**	**3**	**5**
		OR			
9.		Explain the CMSIS organization with a neat diagram.	**4**	**2**	**10**
		UNIT-5			
10.	**a).**	Explain the key debugging features of ARM Cortex-M3.	**5**	**2**	**5**
	b).	What is the Trace System in ARM Cortex-M3? Explain its components and working.	**5**	**1**	**5**
		OR			
11.	**a).**	Discuss how low-power design techniques optimize embedded system performance.	**5**	**2**	**5**
	b).	Explain the working and applications of the SYSTICK timer in ARM Cortex-M3.	**5**	**2**	**5**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE : Questions can be given as A,B splits or as a single Question for 10 marks

					Course Code: B23EC3206
SAGI RAMA KRISHNAM RAJU ENGINEERING COLLEGE (A)					**R23**
III B.Tech. II Semester MODEL QUESTION PAPER					
DATA COMMUNICATIONS AND COMPUTER NETWORKS					
For ECE					
Time: 3 Hrs.					**Max. Marks: 70 M**
Answer Question No.1 compulsorily					
Answer **ONE Question** from **EACH UNIT**					
Assume suitable data if necessary					
					10 x 2 = 20 Marks
			CO	**KL**	**M**
1.	**a).**	List the components of Data communication system	**1**	**1**	**2**
	b).	Explain the purpose of protocol hierarchies	**1**	**1**	**2**
	c).	What is multiplexing? List the types of multiplexing	**2**	**1**	**2**
	d).	Explain character stuffing and bit stuffing	**2**	**1**	**2**
	e).	Compare Pure ALOHA and Slotted AlOHA	**3**	**1**	**2**
	f).	Define Collision	**3**	**1**	**2**
	g).	List the functions of a repeater	**4**	**1**	**2**
	h).	What is the need for a congestion control algorithm? Name any two	**4**	**2**	**2**
	i).	What is the role of DNS in networking	**5**	**2**	**2**
	j).	What is need of port address in transport layer	**5**	**2**	**2**
					5 x 10 =50Marks
		UNIT-1			
2.	**a).**	Differentiate the three categories of Networks LAN, MAN and WAN.	**1**	**3**	**5**
	b).	Compare the functions of Network layer and Data link layer of OSI model in transferring data between source and destination separated by multiple networks.	**1**	**3**	**5**
		OR			
3.	**a).**	Explain different modes of data transmission	**1**	**2**	**5**
	b).	Compare Connection Oriented and Connectionless services	**1**	**3**	**5**
		UNIT-2			
4.	**a).**	Explain the mechanism of Go Back n and Selective Repeat sliding window protocols	**2**	**2**	**5**
	b).	Explain about various types of transmission media	**2**	**2**	**5**
		OR			
5.		The frame received by the receiver is 10111101100. Using the generator polynomial G(x) = + 1, verify if the frame is correct or damaged.	**2**	**3**	**5**

		UNIT-3			
6.	**a).**	Explain 802.11 Wifi architecture	**3**	**2**	**5**
	b).	Derive the efficiency of Slotted ALOHA	**3**	**4**	**5**
		OR			
7.	**a).**	Illustrate the IEEE 802.3 Ethernet standard architecture.	**3**	**3**	**5**
	b).	Explain the concept of Carrier Sense Multiple Access (CSMA) with collision detection.	**3**	**2**	**5**
		UNIT-4			
8.	**a).**	Distinguish the characteristics of virtual circuit and Datagram subnet.	**4**	**3**	**5**
	b).	b). Differentiate the working of ethernet switch and router.	**4**	**3**	**5**
		OR			
9.	**a).**	Explain the operation of Leaky Bucket Algorithm. Determine its advantages over the Token Bucket Algorithm.	**4**	**3**	**5**
	b).	Explain about IPV4 Addressing Scheme.	**4**	**2**	**5**
		UNIT-5			
10.	**a).**	Explain the operation of UDP with the help of its header format. List the applications.	**5**	**3**	**5**
	b).	Explain about elements of Transport protocols.	**5**	**2**	**5**
		OR			
11.	**a).**	Describe the main function of DNS.	**5**	**2**	**5**
	b).	Explain about the World wide web.	**5**	**2**	**5**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE : Questions can be given as A,B splits or as a single Question for 10 marks

					Course Code: B23EC3207
SAGI RAMA KRISHNAM RAJU ENGINEERING COLLEGE (A)					**R23**
III B.Tech. II Semester MODEL QUESTION PAPER					
RADAR ENGINEERING					
For ECE					
Time: 3 Hrs.					**Max. Marks: 70 M**
Answer Question No.1 compulsorily					
Answer **ONE Question** from **EACH UNIT**					
Assume suitable data if necessary					
					10 x 2 = 20 Marks
			CO	**KL**	**M**
1.	**a).**	What do you mean by maximum unambiguous range?	**1**	**2**	**2**
	b).	What is called a false alarm?	**1**	**2**	**2**
	c).	what are the functions of the Duplexer	**2**	**2**	**2**
	d).	what are the functions of the Mixer	**2**	**2**	**2**
	e).	Give the function of STALO and COHO in MTI radars	**3**	**4**	**2**
	f).	What is blind speed and why does it occur in MTI Radar?	**3**	**3**	**2**
	g).	What is the significance of the term "monopulse"?	**4**	**2**	**2**
	h).	Distinguish between "Search mode" and "tracking mode" of a Radar.	**4**	**4**	**2**
	i).	What are the advantages of a Phased Array Radar	**5**	**2**	**2**
	j).	How does the repeater jammer work?	**5**	**3**	**2**
					5 x 10 =50Marks
		UNIT-1			
2.		Draw the block diagram of the radar and explain its working	**1**	**3**	**10**
		OR			
3.	**a).**	Derive the Radar Range Equation.	**1**	**3**	**6**
	b).	What are the System losses of Radar.	**1**	**3**	**4**
		UNIT-2			
4.		Explain in detail about i) Branch type duplexer ii) Balanced type duplexer	**2**	**3**	**10**
		OR			
5.		Explain the various Radar Displays (Scopes)	**2**	**3**	**10**
		UNIT-3			
6.		Illustrate the coherent MTI radar with a neat block diagram and explain the function of each block in detail	**3**	**3**	**10**
		OR			
7.		What is the Doppler effect? A C-band (f T = 5000MHz) Doppler Radar	**3**	**4**	**10**

		is to detect all targets with radial velocities greater than 5 miles per hour and less than 60 miles per hour. What are the minimum and maximum Doppler frequencies which Radar must detect?			
		UNIT-4			
8.		Draw the block diagram of the amplitude comparison monopulse tracking radar in two coordinates and explain its operation.	**4**	**3**	**10**
		OR			
9.	**a).**	Draw the block diagram of the Conical scan tracking radar and explain its operation.	**4**	**3**	**6**
	b).	Compare the Sequential lobing and monopulse tracking radar.	**4**	**4**	**4**
		UNIT-5			
10.		Draw the block schematic diagram of a phased array radar and explain its operation.	**5**	**4**	**10**
		OR			
11.	**a).**	Explain the various techniques that can be used electronically to interfere with Radar performance.	**5**	**4**	**6**
	b).	What are the Electronic counter measures that can be taken to overcome the various techniques that can be used electronically to interfere with Radar performance?	**5**	**4**	**4**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE : Questions can be given as A,B splits or as a single Question for 10 marks

					Course Code: B23EC3208
		SAGI RAMA KRISHNAM RAJU ENGINEERING COLLEGE (A)			**R23**
		III B.Tech. II Semester MODEL QUESTION PAPER			
		MACHINE LEARNING			
		For ECE			
Time: 3 Hrs.					**Max. Marks: 70 M**
		Answer Question No.1 compulsorily			
		Answer **ONE Question** from **EACH UNIT**			
		Assume suitable data if necessary			
					10 x 2 = 20 Marks
			CO	**KL**	**M**
1.	**a).**	Compare Traditional Programming and Machine Learning approaches.	**1**	**2**	**2**
	b).	Distinguish between Quantitative and Qualitative data with examples.	**1**	**2**	**2**
	c).	Give an example for One-Hot-Encoding in feature engineering.	**2**	**3**	**2**
	d).	What is Principal Component Analysis (PCA) used for?	**2**	**2**	**2**
	e).	Give the formula for Linear Regression and explain its components.	**3**	**3**	**2**
	f).	List any four classification algorithms used in Supervised ML.	**3**	**2**	**2**
	g).	What are the differences between Hard and Soft Clustering?	**4**	**2**	**2**
	h).	Define Clustering. Give two real-world applications.	**4**	**1**	**2**
	i).	Mention two advantages of using Cross-Validation.	**5**	**2**	**2**
	j).	List any four evaluation metrics used for regression models.	**5**	**1**	**2**
					5 x 10 =50Marks
		UNIT-1			
2.	**a).**	Explain the evolution and history of Machine Learning.	**1**	**2**	**5**
		Explain the concept of Machine Learning and how it differs from traditional programming with suitable examples.	**1**	**2**	**5**
		OR			
3.	**a).**	Describe quantitative and qualitative data types used in ML with real-world examples.	**1**	**3**	**5**
	b).	Explain Learning by Rote and Learning by Induction. Give an example for each to show the difference.	**1**	**3**	**5**
		UNIT-2			
4.	**a).**	Describe the steps involved in data cleaning and handling missing values and outliers.	**2**	**3**	**5**
	b).	Perform basic Exploratory Data Analysis (EDA) on a given dataset by identifying key patterns or insights and explain how it supports ML model building.	**2**	**3**	**5**
		OR			
5.	**a).**	Using a sample dataset, apply Univariate, Bivariate, and Multivariate	**2**	**3**	**5**

		analysis and interpret the visualizations or findings from each			
	b).	Given a dataset with categorical variables, perform Feature Engineering using One-Hot-Encoding and explain the resulting transformation.	**2**	**3**	**5**
		UNIT-3			
6.	**a).**	Apply any one classification algorithm (e.g., Decision Tree or KNN) on a sample dataset and describe the outcome.	**3**	**3**	**5**
	b).	Given a dataset, identify whether it requires classification or regression and justify your choice with model implementation.	**3**	**3**	**5**
		OR			
7.	**a).**	Use a Random Forest Classifier on a dataset and explain how it improves accuracy compared to a single Decision Tree.	**3**	**3**	**5**
	b).	Train both Decision Tree and Logistic Regression models on a binary classification dataset and compare their confusion matrices.	**3**	**3**	**5**
		UNIT-4			
8.	**a).**	Given a dataset, apply both Hard Clustering (e.g., K-Means) and Soft Clustering (e.g., Gaussian Mixture Model) and compare the results	**4**	**3**	**5**
	b).	Apply K-Means clustering on a sample dataset and visualize the cluster assignments.	**4**	**4**	**5**
		OR			
9.	**a).**	Perform Agglomerative Hierarchical Clustering on a given dataset and represent the result using a dendrogram.	**4**	**3**	**5**
	b).	Apply any unsupervised learning technique (e.g., DBSCAN) on a real-world dataset and discuss practical challenges faced during implementation.	**4**	**3**	**5**
		UNIT-5			
10.	**a).**	Given a confusion matrix for a binary classification problem, analyze how Accuracy, Precision, Recall, and F1-Score are calculated and interpret their significance in evaluating the model.	**5**	**4**	**5**
	b).	Analyze the difference between MSE and RMSE in regression by comparing their impact on model evaluation for datasets with outliers.	**5**	**4**	**5**
		OR			
11.	**a).**	Analyze the role of Stratified K-Fold Cross-Validation in handling imbalanced classification datasets and compare it with simple K-Fold validation.	**5**	**4**	**5**
	b).	Using a heatmap created from a multivariate dataset, analyze the correlations between features and discuss how this influences feature selection in ML models.	**5**	**4**	**5**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE : Questions can be given as A,B splits or as a single Question for 10 marks

					Course Code:B23EC3209
SAGI RAMA KRISHNAM RAJU ENGINEERING COLLEGE (A)					**R23**
III B.Tech. II Semester MODEL QUESTION PAPER					
SMART AND WIRELESS INSTRUMENTATION					
For ECE					
Time: 3 Hrs.					**Max. Marks: 70 M**
Answer Question No.1 compulsorily					
Answer **ONE Question** from **EACH UNIT**					
Assume suitable data if necessary					
					10 x 2 = 20 Marks
			CO	**KL**	**M**
1.	**a).**	List any four classifications of sensors.	**1**	**1**	**2**
	b).	Write short notes on the evolution and history of WSN	**1**	**2**	**2**
	c).	Write a short note on the IMote node architecture.	**2**	**2**	**2**
	d).	Mention any two communication interfaces used in node architecture	**2**	**1**	**2**
	e).	What is source encoding	**3**	**1**	**2**
	f).	List different types of modulation used in WSN	**3**	**1**	**2**
	g).	What is Zigbee communication?	**4**	**1**	**2**
	h).	Write two energy management techniques.	**4**	**2**	**2**
	i).	How are seismic events sensed using WSN?	**5**	**2**	**2**
	j).	List any two WSN applications in healthcare.	**5**	**1**	**2**
					5 x 10 = 50 Marks
		UNIT-1			
2.	**a).**	Explain the concept of Smart Instrumentation and its evolution with suitable examples	**1**	**3**	**5**
	b).	Describe the communication process in a WSN and its challenges	**1**	**3**	**5**
		OR			
3.	**a).**	Explain the various design constraints of a WSN — energy, self-management, and security.	**1**	**3**	**5**
	b).	Examine the aspects of decentralized management and wireless networking in a WSN	**1**	**3**	**5**
		UNIT-2			
4.	**a).**	Explain the architectural overview of a typical node in a WSN.	**2**	**3**	**5**
	b)	Compare microcontrollers, DSPs, ASICs, and FPGAs in node architectures.	**2**	**4**	**5**
		OR			
5	**a).**	Describe the working of the XYZ node architecture with a neat block	**2**	**3**	**5**

		diagram			
	b).	Discuss SPI and I2C communication interfaces used in WSN nodes.	**2**	**3**	**5**
		UNIT-3			
6.	**a).**	Explain the basic components of a wireless digital communication system.	**3**	**3**	**5**
	b).	Discuss information transmission over a channel and error recognition/correction.	**3**	**3**	**5**
		OR			
7.	**a).**	Describe Quadrature Amplitude Modulation with suitable diagrams.	**3**	**3**	**5**
	b).	Explain signal propagation and its challenges in wireless communication systems.	**3**	**3**	**5**
		UNIT-4			
8.	**a).**	Discuss the development of a WSN based on microcontroller and Zigbee.	**4**	**3**	**5**
	b).	Explain various energy harvesting methods and their principles.	**4**	**3**	**5**
		OR			
9.	**a).**	Describe different energy management techniques for battery-powered WSN nodes	**4**	**3**	**5**
	b).	Explain how battery selection is calculated for WSN applications.	**4**	**3**	**5**
		UNIT-5			
10.	**a).**	Explain single and multiple damage detection techniques using natural frequencies and mode shapes.	**5**	**3**	**5**
	b).	Describe precision agriculture and how WSN supports it	**5**	**3**	**5**
		OR			
11.	**a).**	Discuss the role of WSN in traffic control and healthcare monitoring.	**5**	**3**	**5**
	b).	Explain applications of WSN in underground mining and active volcano monitoring	**5**	**3**	**5**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE : Questions can be given as A,B splits or as a single Question for 10 marks

Course Code: B23EC3211					
SAGI RAMA KRISHNAM RAJU ENGINEERING COLLEGE (A)					**R23**
III B.Tech. II Semester MODEL QUESTION PAPER					
DIGITAL VLSI LAYOUT DESIGN					
For ECE					
Time: 3 Hrs.					**Max. Marks: 70 M**
Answer Question No.1 compulsorily					
Answer **ONE Question** from **EACH UNIT**					
Assume suitable data if necessary					
					10 x 2 = 20 Marks
			CO	**KL**	**M**
1.	a).	Briefly explain the role of masks in VLSI layout.	**1**	**2**	**2**
	b).	What is schematic capturing in the layout workflow?	**1**	**1**	**2**
	c).	Define floor-planning in the context of VLSI layout.	**2**	**1**	**2**
	d).	What is the primary goal of placement in IC layout?	**2**	**1**	**2**
	e).	Distinguish between Design Rule Check (DRC) and Layout vs Schematic.	**3**	**3**	**2**
	f).	Briefly explain the function of Electrical Rule Check (ERC).	**3**	**2**	**2**
	g).	What is a digital cell library?	**4**	**1**	**2**
	h).	Explain the concept of an Euler path in digital cell design.	**4**	**2**	**2**
	i).	Why is it important to consider masks and rules during CAD drawing of an inverter?	**5**	**1**	**2**
	j).	Draw the symbol for a NAND gate and state its boolean expression.	**5**	**1**	**2**
					5 x 10 = 50 Marks
		UNIT-1			
2.	**a).**	Explain the complete layout workflow, from schematic capturing to the final drawn layers, highlighting the significance of each stage.	**1**	**2**	**10**
		OR			
3.	**a).**	Describe the importance of understanding masks and their associated rules in VLSI layout.	**1**	**2**	**5**
	b).	Provide an example of how a mask rule might impact the layout of a simple component.	**1**	**2**	**5**
		UNIT-2			
4.	**a).**	Define floor-planning in VLSI layout.	**2**	**1**	**5**
	b).	Explain its importance in achieving an optimal design.	**2**	**2**	**5**
		OR			
5.	**a).**	Explain the concept of routing in VLSI layout.	**2**	**1**	**5**
	b).	Discuss different types of routing techniques used to connect components.	**2**	**3**	**5**

		UNIT-3			
6.	**a).**	Describe the essential components of a Process Design Kit (PDK).	**3**	**3**	**5**
	b).	Explain their role in facilitating VLSI design and verification.	**3**	**2**	**5**
		OR			
7.	**a).**	Explain the purpose of Layout versus Schematic (LVS) verification.	**3**	**2**	**5**
	b).	How does it ensure the correctness of a layout?	**3**	**2**	**5**
		UNIT-4			
8.	**a).**	Explain the Euler path concept.	**4**	**3**	**5**
	b).	how it is applied in the design and routing of digital cells to optimize layout.	**4**	**2**	**5**
		OR			
9.	**a).**	Discuss the guidelines for standard cell layout.	**4**	**2**	**5**
	b).	How do metal spacing grids influence digital cell design?	**4**	**2**	**5**
		UNIT-5			
10.	**a).**	Draw the CAD layout of a CMOS Inverter, clearly indicating the different mask layers involved.	**5**	**3**	**10**
		OR			
11.	**a).**	Draw the CAD layout for an XOR gate, specifying the masks and rules that would be applied in a typical technology.	**5**	**3**	**10**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE : Questions can be given as A,B splits or as a single Question for 10 marks

					Course Code: B23EC3212
		SAGI RAMA KRISHNAM RAJU ENGINEERING COLLEGE (A)			**R23**
		III B.Tech. II Semester MODEL QUESTION PAPER			
		REAL TIME OPERATING SYSTEMS			
		For ECE			
Time: 3 Hrs.					**Max. Marks: 70 M**
		Answer Question No.1 compulsorily			
		Answer **ONE Question** from **EACH UNIT**			
		Assume suitable data if necessary			
					10 x 2 = 20 Marks
			CO	**KL**	**M**
1.	**a).**	Differentiate between hard real-time and soft real-time systems.	**1**	**2**	**2**
	b).	What is a context switch in RTOS?	**1**	**1**	**2**
	c).	Define a semaphore and explain its role in synchronization.	**2**	**2**	**2**
	d).	What are the key differences between binary semaphores and counting semaphores?	**2**	**2**	**2**
	e).	What are the key differences between binary semaphores and counting semaphores?	**3**	**2**	**2**
	f).	Explain the function of an event register in real-time applications.	**3**	**1**	**2**
	g).	What is the difference between an exception and an interrupt ?	**4**	**2**	**2**
	h).	Explain the role of a timer interrupt service routine (ISR) in RTOS.	**4**	**1**	**2**
	i).	What is dynamic memory allocation in embedded systems?	**5**	**1**	**2**
	j).	Define barrier synchronization and explain its significance in RTOS	**5**	**1**	**2**
					5 x 10 =50Marks
		UNIT-1			
2.	**a).**	Explain the key characteristics of an RTOS that make it suitable for real-time applications.	**1**	**2**	**5**
	b).	Describe the role of a scheduler in RTOS and explain the difference between preemptive priority-based scheduling and round-robin scheduling.	**1**	**2**	**5**
		OR			
3.	**a).**	Explain the concept of multitasking in RTOS and describe its benefits and challenges.	**1**	**2**	**5**
	b).	Discuss the importance of RTOS objects and services in managing real-time tasks effectively.	**1**	**2**	**5**
		UNIT-2			
4.	**a).**	Explain the various task states in RTOS and describe how task scheduling is managed.	**2**	**2**	**5**
	b).	Describe briefly the structure of a message queue in RTOS	**2**	**2**	**5**
		OR			

5.	**a).**	Explain the Typical task operations	**2**	**2**	**5**
	b).	Discuss the in-detail about mutual exclusion (mutex) semaphores	**2**	**2**	**5**
		UNIT-3			
6.	**a).**	Describe the structure and functionality of a pipe in RTOS. How does it improve data communication between tasks?	**3**	**2**	**5**
	b).	Explain the role of signals in RTOS. Explain signal control blocks	**3**	**2**	**5**
		OR			
7.	**a).**	Describe the typical operations of pipes	**3**	**2**	**5**
	b).	Discuss event register operations and uses of event registers.	**3**	**2**	**5**
		UNIT-4			
8.	**a).**	Explain the steps involved in handling a general exception in RTOS.	**4**	**2**	**5**
	b).	Discuss about programmable interval timer	**4**	**2**	**5**
		OR			
9.	**a).**	Discuss about Programmable Interrupt Controllers and External Interrupts	**4**	**2**	**5**
	b).	Discuss the role of real-time clocks and system clocks in managing time-sensitive tasks in RTOS.	**4**	**2**	**5**
		UNIT-5			
10.	**a).**	Classify Port-Mapped vs. Memory-Mapped I/O and DMA	**5**	**3**	**5**
	b).	Explain the concept of Fixed-Size Memory Management in Embedded Systems	**5**	**2**	**5**
		OR			
11.	**a).**	Explain about Hardware Memory Management Units	**5**	**2**	**5**
	b).	Discuss about Resource Synchronization	**5**	**3**	**5**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE : Questions can be given as A,B splits or as a single Question for 10 marks

					Course Code: B23EC3213
		SAGI RAMA KRISHNAM RAJU ENGINEERING COLLEGE (A)			**R23**
		III B.Tech. II Semester MODEL QUESTION PAPER			
		CRYPTOGRAPHY AND NETWORK SECURITY			
		For ECE			
Time: 3 Hrs.					**Max. Marks: 70 M**
		Answer Question No.1 compulsorily			
		Answer **ONE Question** from **EACH UNIT**			
		Assume suitable data if necessary			
					10 x 2 = 20 Marks
			CO	**KL**	**M**
1.	**a).**	What is the difference between passive and active security attacks?	**1**	**2**	**2**
	b).	What are the key principles to consider when designing a secure block cipher?	**1**	**1**	**2**
	c).	Differentiate conventional (symmetric) from public key (asymmetric) encryption.	**2**	**2**	**2**
	d).	What are the different modes of operation in DES?	**2**	**1**	**2**
	e).	How does Diffie-Hellman key exchange achieve security?	**3**	**2**	**2**
	f).	What is meant by one-way property in hash function?	**3**	**2**	**2**
	g).	What is the purpose of the Authentication Header (AH) in IPsec?	**4**	**2**	**2**
	h).	How does SSL/TLS ensure secure communication over the web?	**4**	**2**	**2**
	i).	List out the design goals of firewalls.	**5**	**1**	**2**
	j).	What is the role of consensus mechanisms in blockchain?	**5**	**2**	**2**
					5 x 10 = 50 Marks
		UNIT-1			
2.	**a).**	Differentiate Active attacks and Passive attacks.	**1**	**2**	**5**
	b).	Explain about Traditional Block cipher Structure.	**1**	**2**	**5**
		OR			
3.	**a).**	What is mono alphabetic cipher? How it differs from Caesar cipher.	**1**	**2**	**5**
	b).	Explain Block cipher design principles.	**1**	**2**	**5**
		UNIT-2			
4.	**a).**	Perform Encryption and Decryption using RSA algorithm for p=17,q=11,e=7,M=88.	**2**	**3**	**5**
	b).	Explain the structure of AES algorithm with neat diagram and describe the steps in AES encryption.	**2**	**2**	**5**
		OR			
5.	**a).**	Find the secret key shared between User A and User B using Diffie Hellman Key exchange algorithm for the following: q=97, a=5, the	**2**	**3**	**5**

		private keys $X_A = 36$, $X_B = 58$.			
	b).	Explain Block Cipher modes of operations.	**2**	**2**	**5**
		UNIT-3			
6.	**a).**	Illustrate digital signature algorithm with neat diagram and explain how to sign and verify using DSS algorithm.	**3**	**3**	**5**
	b).	Differentiate between HMAC and CMAC.	**3**	**2**	**5**
		OR			
7.	**a).**	List and explain various steps of SHA in detail with neat diagram.	**3**	**2**	**5**
	b).	Describe Kerberos with steps to grant the ticket.	**3**	**2**	**5**
		UNIT-4			
8.	**a).**	Describe IP sec architecture with neat diagram.	**4**	**3**	**5**
	b).	Discuss the services provided by PGP with neat diagram.	**4**	**2**	**5**
		OR			
9.	**a).**	Discuss in detail about SSL/TLS.	**4**	**3**	**5**
	b).	Explain Web security requirements	**4**	**2**	**5**
		UNIT-5			
10.	**a).**	Explain key elements in Blockchain technology.	**5**	**3**	**5**
	b).	Explain about different types of firewalls.	**5**	**2**	**5**
		OR			
11.	**a).**	Explain how firewalls are configured.	**5**	**3**	**5**
	b).	Describe how Blockchain technology is used in smart contracts.	**5**	**2**	**5**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE : Questions can be given as A,B splits or as a single Question for 10 marks

					Course Code: B23EC3214
		SAGI RAMA KRISHNAM RAJU ENGINEERING COLLEGE (A)			**R23**
		III B.Tech. II Semester MODEL QUESTION PAPER			
		MICROWAVE ENGINEERING			
		For ECE			
Time: 3 Hrs.					**Max. Marks: 70 M**
		Answer Question No.1 compulsorily			
		Answer **ONE Question** from **EACH UNIT**			
		Assume suitable data if necessary			
					10 x 2 = 20 Marks
			CO	**KL**	**M**
1.	**a).**	List the microwave applications.	**1**	**2**	**2**
	b).	Explain the probe and Loop.	**1**	**3**	**2**
	c).	List out the scattering properties.	**2**	**2**	**2**
	d).	Explain the significance of scattering matrix.	**2**	**2**	**2**
	e).	Classify microwave tubes.	**3**	**1**	**2**
	f).	Explain the slow wave structures.	**3**	**2**	**2**
	g).	Explain the negative resistance phenomenon.	**4**	**2**	**2**
	h).	What are the applications of solid sate devices?	**4**	**1**	**2**
	i).	List the blocks of microwave bench setup.	**5**	**2**	**2**
	j).	Define the VSWR?	**5**	**1**	**2**
					5 x 10 = 50 Marks
		UNIT-1			
2.	**a).**	Explain the operation of a Magic Tee and its applications in detail	**1**	**3**	**5**
	b).	State the principle of operation of Directional coupler. Explain the operation of two hole directional coupler in detail.	**1**	**3**	**5**
		OR			
3.	**a).**	Explain the operation of circulator	**1**	**4**	**6**
	b).	State Faraday rotation principle. Explain the operation of the isolator.	**1**	**3**	**4**
		UNIT-2			
4.	**a).**	What is a scattering matrix? Write the properties of a scattering matrix	**2**	**3**	**5**
	b).	Derive the S-parameters for Magic Tee.	**2**	**3**	**5**
		OR			
5.	**a).**	Show that the 'S' matrix of a perfectly matched 2-port network is $\begin{bmatrix} 0 & 0 \\ 1 & 0 \end{bmatrix}$	**2**	**3**	**5**
	b).	Explain the operations of directional coupler with the help s-parameters	**2**	**3**	**5**
		UNIT-3			

6.	**a).**	Explain the limitations of conventional tubes at Microwave frequencies in detail	**3**	**3**	**5**
	b).	Explain the working of Reflex klystron with neat diagram	**3**	**3**	**5**
		OR			
7.	**a).**	Explain the working of Helix travelling wave tube with neat diagram	**3**	**3**	**5**
	b).	Explain the working of 8-cavity Magnetron with neat diagram	**3**	**3**	**5**
		UNIT-4			
8.	**a).**	Explain in detail the principle of operation of GUNN diode and detail different modes of operation of gunn diode.	**4**	**3**	**5**
	b).	Explain the operation IMPATTdiode with suitable diagrams.	**4**	**3**	**5**
		OR			
9.	**a).**	Explain the operation TRAPATT diode with suitable diagrams	**4**	**3**	**5**
	b).	Explain the operation TUNNEL diode with suitable diagrams	**4**	**3**	**5**
		UNIT-5			
10.	**a).**	Explain the procedure with a neat diagram to measure the frequency and guide wave length	**5**	**3**	**5**
	b).	Explain the procedure for measurement of low and high VSWR with block diagram.	**5**	**3**	**5**
		OR			
11.		Draw the Block Diagram of Microwave bench setup and explain each block	**5**	**3**	**10**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE : Questions can be given as A,B splits or as a single Question for 10 marks

					Course Code: B23EC3215
		SAGI RAMA KRISHNAM RAJU ENGINEERING COLLEGE (A)			**R23**
		III B.Tech. II Semester MODEL QUESTION PAPER			
		ANALOG IC DESIGN			
		For ECE			
Time: 3 Hrs.					**Max. Marks: 70 M**
		Answer Question No.1 compulsorily			
		Answer **ONE Question** from **EACH UNIT**			
		Assume suitable data if necessary			
					10 x 2 = 20 Marks
			CO	**KL**	**M**
1.	**a).**	What are the key parameters in a small-signal MOS transistor model?	**1**	**2**	**2**
	b).	Define sub-threshold conduction in a MOSFET.	**1**	**2**	**2**
	c).	What is the purpose of a beta helper in a current mirror circuit?	**2**	**2**	**2**
	d).	List two advantages of using a cascode current mirror.	**2**	**3**	**2**
	e).	What is the role of compensation in operational amplifier design?	**3**	**2**	**2**
	f).	Mention two differences between a differential amplifier and an inverter.	**3**	**3**	**2**
	g).	Define the term hysteresis in the context of comparators.	**4**	**2**	**2**
	h).	What is the key difference between a comparator and an operational amplifier?	**4**	**3**	**2**
	i).	What is a Voltage-Controlled Oscillator (VCO)?	**5**	**2**	**2**
	j).	Name two applications of Phase-Locked Loops.	**5**	**2**	**2**
					5 x 10 = 50 Marks
		UNIT-1			
2.	**a).**	Explain the significance of passive components in CMOS technology.	**1**	**2**	**5**
	b).	Describe the layout considerations in integrated circuits for MOS design	**1**	**2**	**5**
		OR			
3.	**a).**	Analyze the small-signal model of a MOS transistor for low-frequency applications.	**1**	**3**	**6**
	b).	Compare different computer simulation models used for MOS device analysis.	**1**	**2**	**4**
		UNIT-2			
4.	**a).**	Explain the function of a MOS switch and its practical limitations.	**2**	**2**	**5**
	b).	Describe how a current mirror with beta helper improves performance.	**2**	**2**	**5**
		OR			

5.	**a).**	Analyze the performance of a cascode current mirror in terms of output resistance and compliance voltage	**2**	**3**	**5**
	b).	Explain the principle of operation of a temperature-independent bandgap reference circuit	**2**	**2**	**5**
		UNIT-3			
6.	**a).**	Describe the operation of a differential amplifier and list its key performance parameters	**3**	**2**	**5**
	b).	Analyze the cascode operational amplifier configuration and explain how it improves power supply rejection ratio (PSRR).	**3**	**3**	**5**
		OR			
7.	**a).**	Explain the compensation techniques used in two-stage CMOS operational amplifiers.	**3**	**2**	**5**
	b).	Analyze the high gain amplifier architecture and its significance in analog ICs	**3**	**3**	**5**
		UNIT-4			
8.	**a).**	Define the term comparator and list its important specifications	**4**	**2**	**5**
	b).	Analyze the design improvements to enhance speed and accuracy in open-loop comparators.	**4**	**3**	**5**
		OR			
9.	**a).**	Differentiate between two-stage and other open-loop comparators.	**4**	**3**	**5**
	b).	Explain how discrete-time comparators operate and where they are used.	**4**	**2**	**5**
		UNIT-5			
10.	**a).**	Explain the basic principle and frequency calculation of a ring oscillator.	**5**	**2**	**5**
	b).	Compare LC and ring oscillators in terms of phase noise and frequency stability.	**5**	**3**	**5**
		OR			
11.	**a).**	Describe the operation of a simple PLL and its building blocks.	**5**	**2**	**6**
	b).	Design a basic charge-pump PLL and analyze its non-ideal effects like jitter and lock time.	**5**	**4**	**4**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE : Questions can be given as A,B splits or as a single Question for 10 marks

					Course Code: B23EC3216
		SAGI RAMA KRISHNAM RAJU ENGINEERING COLLEGE (A)			**R23**
		III B.Tech. II Semester MODEL QUESTION PAPER			
		SOFT COMPUTING TECHNIQUES			
		For ECE			
Time: 3 Hrs.					**Max. Marks: 70 M**
		Answer Question No.1 compulsorily			
		Answer **ONE Question** from **EACH UNIT**			
		Assume suitable data if necessary			
					10 x 2 = 20 Marks
			CO	**KL**	**M**
1.	**a).**	Define intelligent control and mention any two approaches used in it.	**1**	**1**	**2**
	b).	What is a rule-based system? Give an example.	**1**	**2**	**2**
	c).	Define an Artificial Neural Network (ANN) and mention its basic components.	**2**	**1**	**2**
	d).	What is the McCulloch-Pitts neuron model? State its significance.	**2**	**2**	**2**
	e).	Differentiate between crisp sets and fuzzy sets with an example.	**3**	**2**	**2**
	f).	What are the main steps involved in fuzzy logic control?	**3**	**2**	**2**
	g).	How does the selection process work in a Genetic Algorithm?	**4**	**2**	**2**
	h).	What is the role of crossover and mutation in Genetic Algorithms?	**4**	**2**	**2**
	i).	What are the advantages of using Genetic Algorithms in power system optimization?	**5**	**2**	**2**
	j).	What is the role of the MATLAB Neural Network Toolbox in system identification?	**5**	**2**	**2**
					5 x 10 = 50 Marks
		UNIT-1			
2.	**a).**	Describe the architecture of an intelligent control system with a neat diagram.	**1**	**3**	**5**
	b).	What is a symbolic reasoning system? Explain its significance in AI-based control systems.	**1**	**3**	**5**
		OR			
3.	**a).**	Explain the role of knowledge representation in intelligent control with an example.	**1**	**3**	**5**
	b).	Describe how symbolic reasoning systems are applied in intelligent control.	**1**	**3**	**5**
		UNIT-2			
4.	**a).**	Explain the McCulloch-Pitts neuron model with its structure, working principle, and significance in Artificial Neural Networks.	**2**	**2**	**5**
	b).	Explain the basic mathematical model of an Artificial Neural Network	**2**	**3**	**5**

		(ANN) with a suitable example.			
		OR			
5.	**a).**	Compare Adaline and Madaline networks with respect to their architecture and learning rules.	**2**	**3**	**5**
	b).	Describe the architecture of a Feed-forward Multilayer Perceptron and its applications.	**2**	**3**	**5**
		UNIT-3			
6.	**a).**	Explain the process of fuzzification and defuzzification in fuzzy logic control.	**3**	**2**	**5**
	b).	Describe how fuzzy modeling is applied for controlling nonlinear systems.	**3**	**3**	**5**
		OR			
7.	**a).**	Illustrate the structure of a fuzzy logic controller with a block diagram.	**3**	**3**	**5**
	b).	Describe the working of a self-organizing fuzzy logic control system with an example.	**3**	**3**	**5**
		UNIT-4			
8.	**a).**	Describe the role of selection, crossover, and mutation in Genetic Algorithms.	**4**	**2**	**5**
	b).	Describe the working principle of Tabu Search with an example.	**4**	**3**	**5**
		OR			
9.	**a).**	How do Genetic Algorithms differ from traditional optimization techniques?	**4**	**2**	**5**
	b).	Illustrate the concept of Ant Colony Optimization (ACO) and its real-world applications.	**4**	**3**	**5**
		UNIT-5			
10.		Analyze the role of Genetic Algorithms in optimizing power system performance. Compare GA-based optimization with conventional techniques and provide a case study to support your analysis.	**5**	**4**	**10**
		OR			
11.	**a).**	Illustrate the process of implementing a fuzzy logic controller using MATLAB fuzzy-logic toolbox.	**5**	**3**	**5**
	b).	Demonstrate how self-organizing neural networks can be used for system control applications.	**5**	**3**	**5**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

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